SCT ASIC PRR Document

SCT Barrel Module : Electrical Performance

Abstract

This document summarises the measured electrical readout performance of barrel modules in the laboratory, in beam tests at CERN and KEK and in the SCT system test at CERN.

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1 SCOPE OF THE DOCUMENT

This document summarises results on the electrical performance of barrel modules read out with the ABCD2T, ABCD3T and the current ABCD3T-A versions of the SCT binary ASICs. It includes

- Noise occupancy versus binary threshold and extracted noise for modules read out individually in the laboratory, both before and after irradiation to a fluence of $3x10^{14}$ pcm^{-2} 24 GeV/c protons.
- Tracking efficiency, charge collection and resolution measurements for both non-irradiated and irradiated modules as measured in test beams at CERN and at KEK.
- First results from an assembly of 15 modules mounted together on a barrel sector in the SCT system test at CERN.

2 PERFORMANCE GOALS

The anticipated performance of SCT barrel modules as recorded in the Inner Detector TDR in 1997 was:

- Signal:noise of about 14:1 pre-irradiation, reducing to about 11.5:1 after 10 years of operation in ATLAS (Figure 11-36, page 435)
- Noise occupancy < $5x10^{-4}$
- Tracking efficiency > 99%

Much has changed in the intervening 4 years, including the detector type (p-in-n rather than n-in-n) and specification, and the evolution of the ABCD ASIC. Nevertheless, the noise occupancy and tracking efficiency specifications remain as the electrical performance goals of the barrel modules.

3 AVAILABLE ELECTRICAL MODULES

The number of electrical barrel modules so far constructed by the SCT has been limited by the supply of ASICs. For this reason data are included from modules constructed with previous versions of the ASIC - the ABCD2T and ABCD3T, as well as the current ABCD3T-A. The modules from which results have been obtained are listed in Table 1.

Module ID	ASIC type	Detector type	Irradiated	Data		
				Lab	Test beam	System Test
K3103	ABCD2T	HP <111>	No	√	√ (KEK)	√
K3104	ABCD2T	HP <111>	No	√		√
K3111	ABCD2T	HP <111>	No	√		
K3112	ABCD2T	HP <100>	No	√	√ (CERN)	√
K3113	ABCD2T	HP <100>	Detectors	√	√ (CERN)	
RLT5	ABCD2T	HP <111> 325μm thick	No	√	√ (CERN)	
RLT4	ABCD2T	HP <111> 325μm thick	Yes	√	√ (CERN)	
RLT9	ABCD2T	HP <111>	Detectors	√	√ (CERN)	
RLT10	ABCD2T	HP <100>	Detectors	√	√ (CERN)	
RLK6	ABCD2T	HP <111>	No	√	√ (CERN)	
Scand1	ABCD2T	Sintef <100>	No	√	√ (CERN)	√
20220170100004	ABCD3T	HP <111>	No	√		√
20220170100011	ABCD3T	HP <100>	No	√	√ (KEK)	√
20220170100022	ABCD3T (thinned and metallised)	HP <100>	No	√	√ (KEK)	√
20220170100003	ABCD3T	HP <100>	Yes	√	√ (KEK)	
20220170100026	ABCD3T	HP <100>	No	√		√
20220170100001	ABCD3T	HP <111>	Yes	√		
20220170100008	ABCD3T (attached with non-conducting glue)	HP <111>	No	√		√
20220170100009	ABCD3T	HP <111>	No	√		√
20220170100020	ABCD3T-A	HP <100>	Yes	√		
20220170100037	ABCD3T-A	HP <100>	Yes	√		
20220170100016	ABCD3T-A	HP <111>	No	√		
20220170100018	ABCD3T-A	HP <111>	No	√		√
20220170100019	ABCD3T-A	HP <111>	No	√		√
20220170100035	ABCD3T-A	HP <100>	No	√		√
20220170100036	ABCD3T-A	HP <100>	No	√		√
20220170100029	ABCD3T-A	HP <111>	No	√		√

Table 1: SCT Barrel Electrical Modules Constructed and Tested as at 1st June 2001

4 RESULTS FROM INDIVIDUAL MODULES

The ASICs are powered with the prototype SCT low voltage power supply, SCTLV2, and readout electrically via an SCT CLOAC-MuSTARD-SLOG system[1]. The electrical test procedures are outlined in Appendix 1.

4.1 Noise and Noise Occupancy at 1fC Threshold for Unirradiated Modules

The noise and noise occupancy are quoted for the modules with ABCD3T and ABCD3T-A ASICs. Non-linearity of the ABCD2T on-chip calibration gives rise to some uncertainty in determining absolute noise values for these modules.

The noise of the ASIC decreases as the temperature is reduced The standard laboratory measurements are made with the hybrid temperature at about 27^{o}C. At this temperature, the measured noise for the ABCD3T modules is in the region of 1400-1700 ENC. This is illustrated in Figure 1, which shows the average noise values for each of the 12 readout ASICs on nine of the ABCD3T(-A) modules.

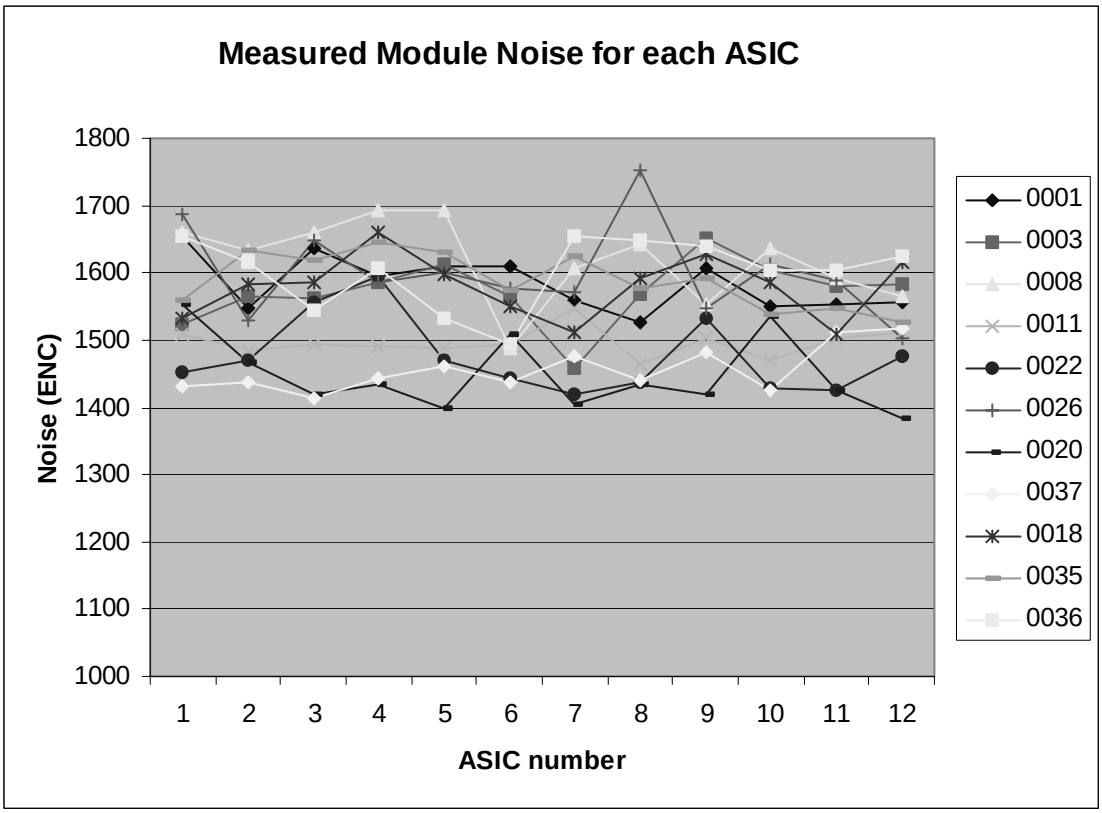

Figure 1: Measured noise (ENC) on each of the 12 ASICs of nine of the modules made with ABCD3T or ABCD3T-A ASICs. The temperature of the hybrid was about 27^{o}C. Each curve is labelled with the four least significant digits of the corresponding module number.

[1] http://sct.home.cern.ch/sct/sctdaq.html

At the SCT operating temperature of ~0°C on the hybrid, the noise is reduced to typically about 1350 ENC for the ABCD3T modules for cold operation. This corresponds to an expected signal:noise value of better than 14:1, thus satisfying the pre-irradiation performance goal of section 2. Signal:noise values for modules as measured in a test beam are consistent with this expectation, and presented in section 5.

The noise of each individual readout channels of an ABCD3T-A module, operated warm, is shown in Figure 2. A uniform noise distribution is seen, apart from a single channel on the module that is bonded to only a 6 cm length of detector.

The SCT design goal is to set the ASIC single-strip binary readout threshold at 1fC, to ensure high tracking efficiency for particles traversing the silicon at inclined angles, depositing charge on more than one readout strip. The noise occupancy of the individual unirradiated modules at this threshold, even when operated warm, is typically ~10^{-5} (that is, < 10^{-4}), which is satisfactory for the SCT (section 2). This is illustrated in Figure 3.

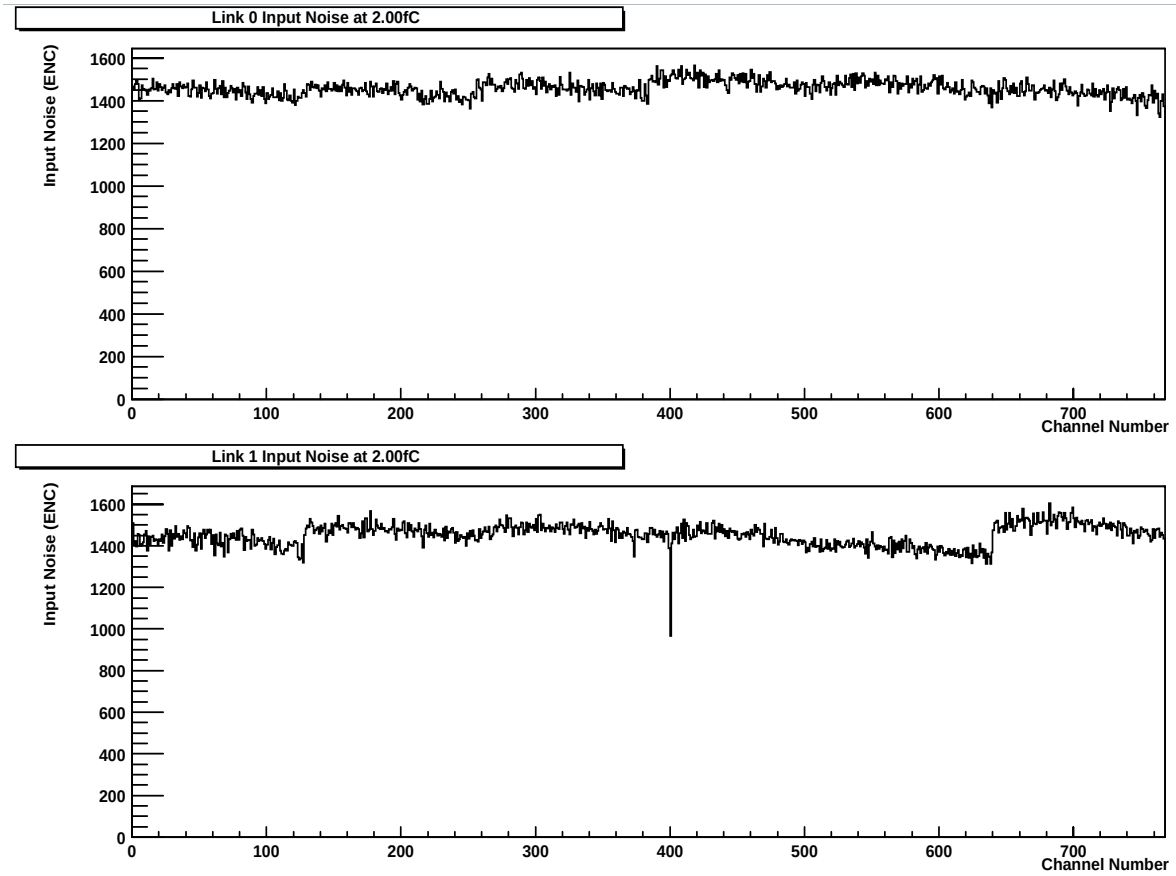

Figure 2: Measured noise values (ENC) on all channels of ABCD3T-A module 20220170100018

4.2 Uniformity of Threshold

Good channel to channel uniformity of the nominal 1fC threshold is essential for operation of a binary readout system. This is ensured through the ASIC threshold correction circuit, where each channel is provided with a trim DAC of 4 bit resolution with four selectable ranges. The first range (0 mV – 60 mV) is used pre-irradiation, which gives a maximum channel to channel variation of 4mV (or ~ 0.08 fC). This is to be compared with the noise value of ~ 0.25 fC. The effect of this channel to channel threshold spread is to give a contribution to the noise occupancy at 1fC equivalent to less than a 1% increase in the intrinsic channel noise.

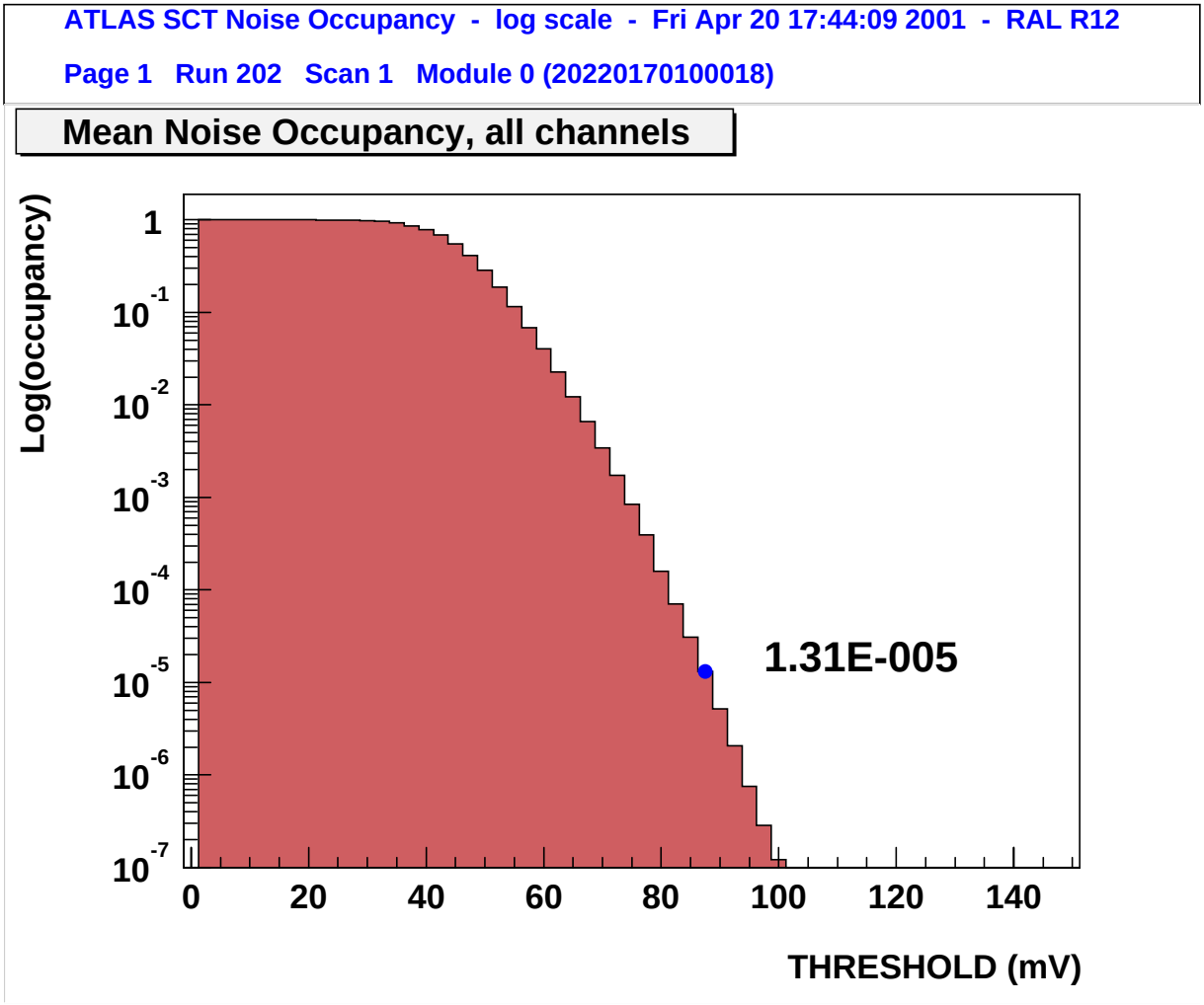

Figure 3: Mean noise occupancy of all channels of ABCD3T-A module 20220170100018, measured warm. The noise occupancy at 1fC threshold is 1.31x10^{-5}.

4.3 Module Stability

Figure 4 shows example plots of occupancy versus threshold for all individual channels from the first readout side of the ABCD3T-A module 20220170100018. We take the smoothness and regularity of these curves as a very sensitive test of the intrinsic stability of a module. The data of Figure 4 show good regularity. In general, with the ABCD3T(-A) ASICs and 220nF V_{cc} and V_{dd} decoupling capacitors on the hybrid, some small irregularities are seen in these 'S-curves' for typically up to four chips on a module, predominantly on the second readout side. This is illustrated in Figure 5, showing this second readout side for the module 20220170100018, where some irregularities appear for the last two ASICs. It should be noted that these effects occur below 0fC threshold, and create no apparent instability in the modules under normal operating conditions.

4.4 Timewalk

The ASIC requirement is that the timewalk should be <16 ns. Here timewalk is defined as the maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1fC. Figure 6 shows measured data for the ABCD3T-A module 20220170100018. The top row of curves shows time in strobe delay units versus injected charge (fC) for each ASIC and the bottom row the timewalk distribution in nsec of the channels of each of the readout chips of the first side. The specification is satisfied for all channels.

4.5 Noise and Noise Occupancy at 1fC Threshold for Irradiated Modules

Results are so far available for two ABCD3T modules (20220170100001 and 3) and two ABCD3T-A modules (20220170100020 and 37) that have been fully irradiated at the CERN PS to a fluence of $3x10^{14}$ pcm^{-2} 24 GeV/c protons. For these, the average measured ASIC noise value when operated cold, with the hybrid around 0^oC, is in the range 1800 ENC to 2060 ENC.

As will be illustrated through the test beam data of section 5, the charge collection efficiency of the irradiated silicon is close to 100% at bias voltages above about 400V. Thus the signal:noise value found for fully irradiated barrel modules is in the region of 10:1 at the SCT operating temperature. This is lower than the target (because of the higher noise). However, noise occupancy at 1fC threshold as measured in the laboratory and test beam is about $2\text{-}3x10^{-4}$. It is thus anticipated that the 1fC threshold can be maintained post-irradiation, to provide maximum tracking efficiency after 10 years of ATLAS operation.

After the maximum fluence, the ASICs may be operated with a very safe margin using the coarsest trim DAC range, trim range 3. After irradiation this range is decreased (typically 0 mV – 190 mV) giving maximum channel to channel variation at the 12mV bin level. This gives a contribution to the noise occupancy equivalent to a ~ 4% increase in noise.

In the ABCD3T, all trim DAC ranges could not be selected reliably after irradiation. This was corrected in the ABCD3T-A version of the chip. The ABCD3T-A modules 20220170100020 and 20220170100037 both have fully functional trim circuitry after exposure to the full dose of $3x10^{14}$ pcm^{-2} 24 GeV/c protons. Figure 7 illustrates the functionality of all the trim DAC ranges for the second readout side of module 20220170100020. The channels can in fact be aligned using trim range 2. The corresponding trim DAC settings and the resultant trimmed thresholds are shown in Figure 8.

The measured post-irradiation noise occupancy as a function of threshold for all channels on the two sides of module 2022017010037 is shown in Figure 9, with channels aligned using trim range 2. A uniform and satisfactory performance is seen across all channels of the module.

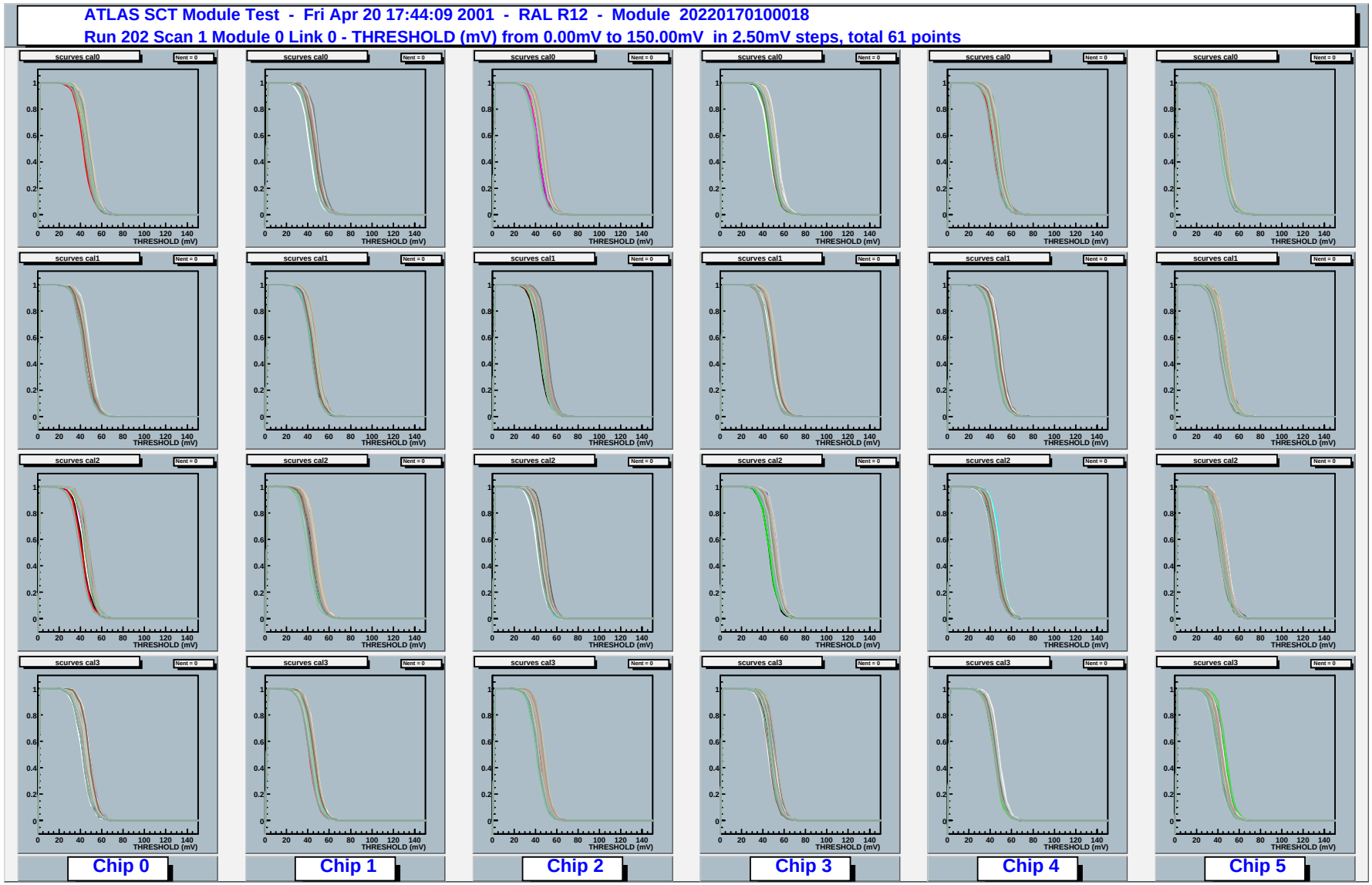

Figure 4: Curves of occupancy versus threshold superimposed for every readout channel of the first readout side of an ABCD3T-A module. Every fourth channel (32 in total) of each ASIC appears in each of the boxes.

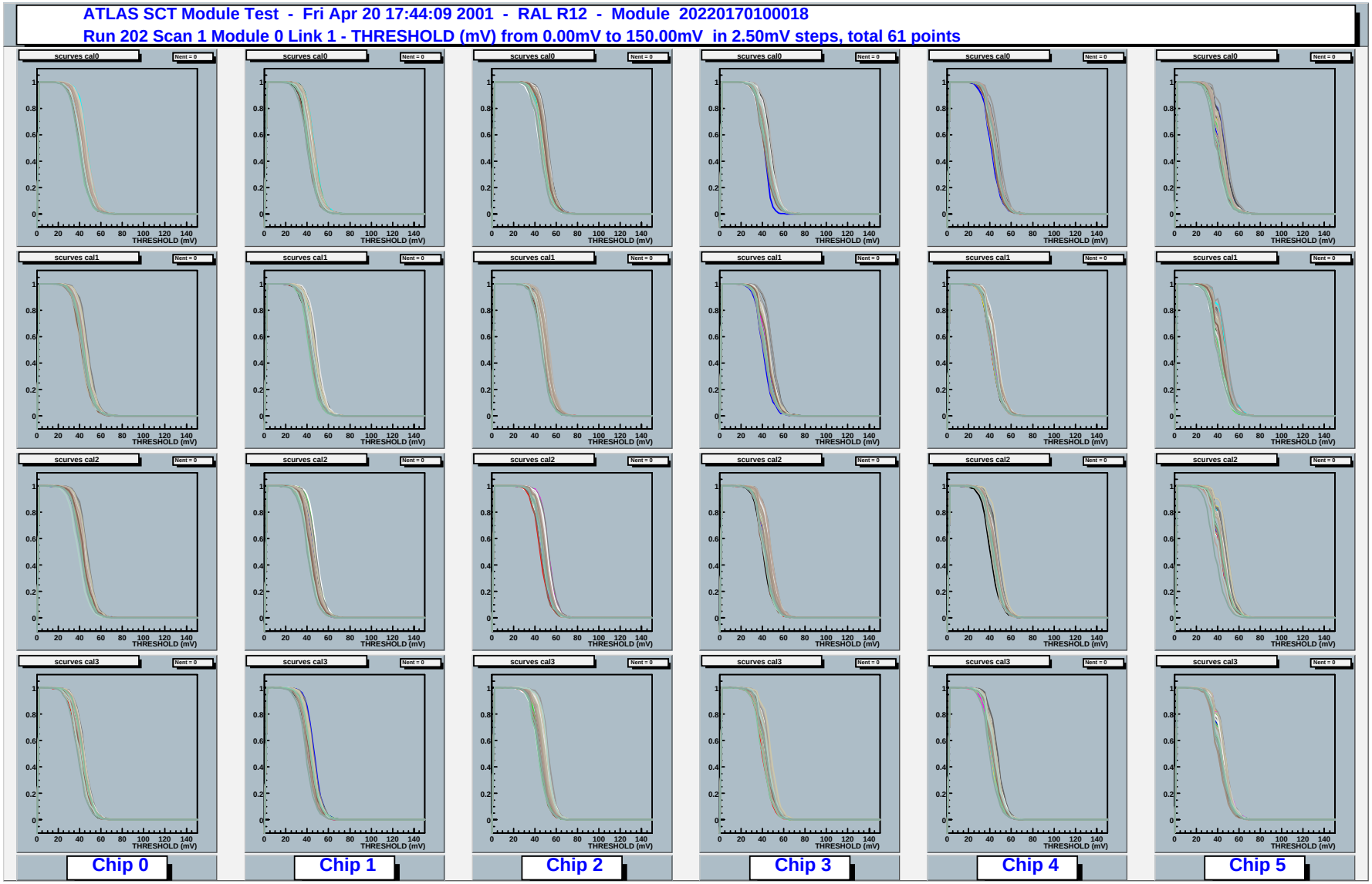

Figure 5: Curves of occupancy versus threshold superimposed for every readout channel of the second readout side of an ABCD3T-A module. Every fourth channel (32 in total) of each ASIC appears in each of the boxes.

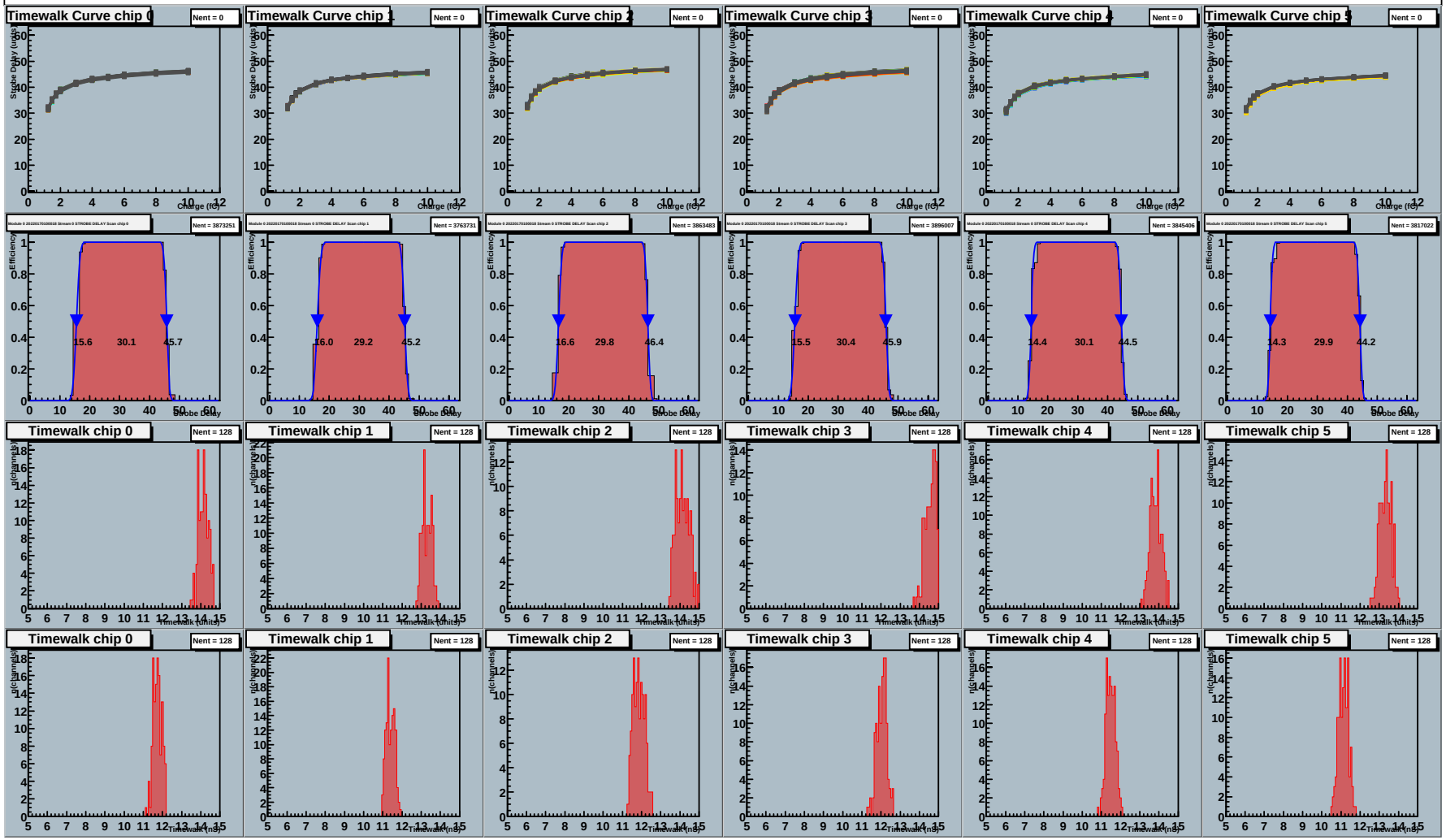

Figure 6: Timewalk curves for the first readout side of an ABCD3T-A module.

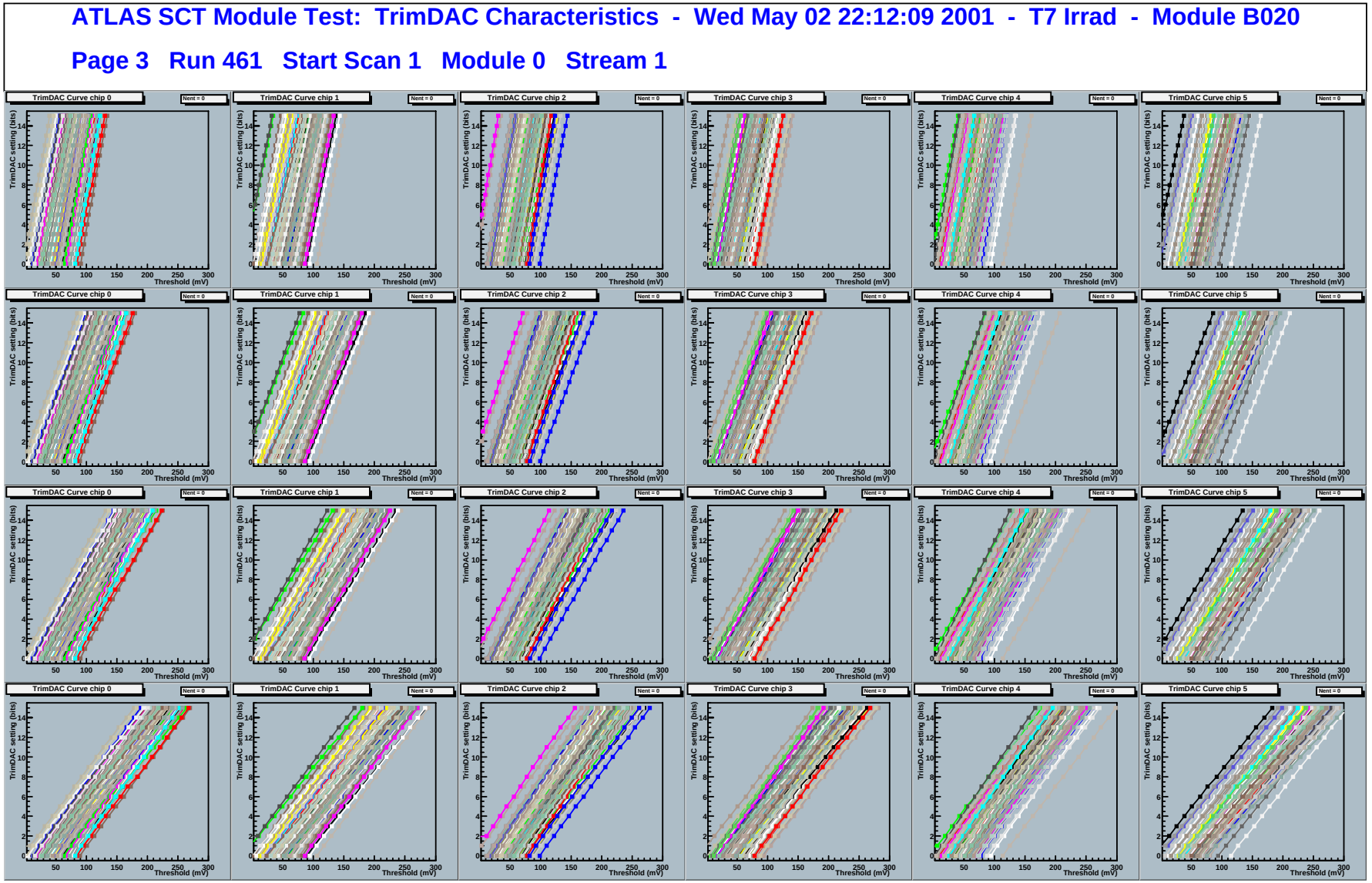

Figure 7: Trim DAC setting versus threshold for each of the 6 ASICs (horizontally) of the second readout side of module 20220170100020 after irradiation to $3x10^{14}$ pcm^{-2} for each of the 4 trim DAC ranges (vertically).

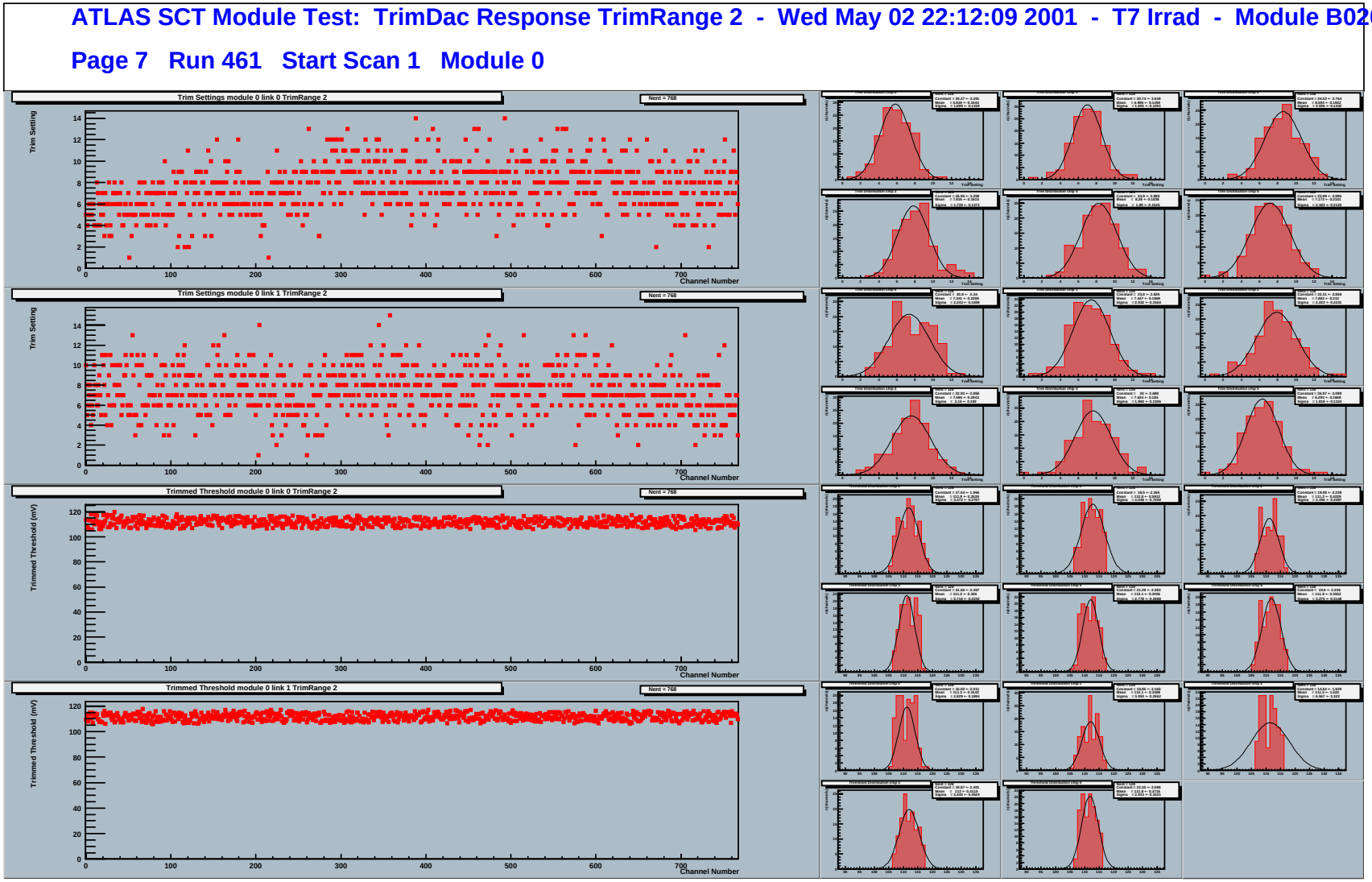

Figure 8: Trim DAC setting versus channel number (upper two rows) and trimmed threshold versus channel number (lower two rows) for module 20220170100020 after irradiation to $3x10^{14}$ pcm^{-2}. The right hand plots show the distribution of the variable for each ASIC on the second readout side of the module

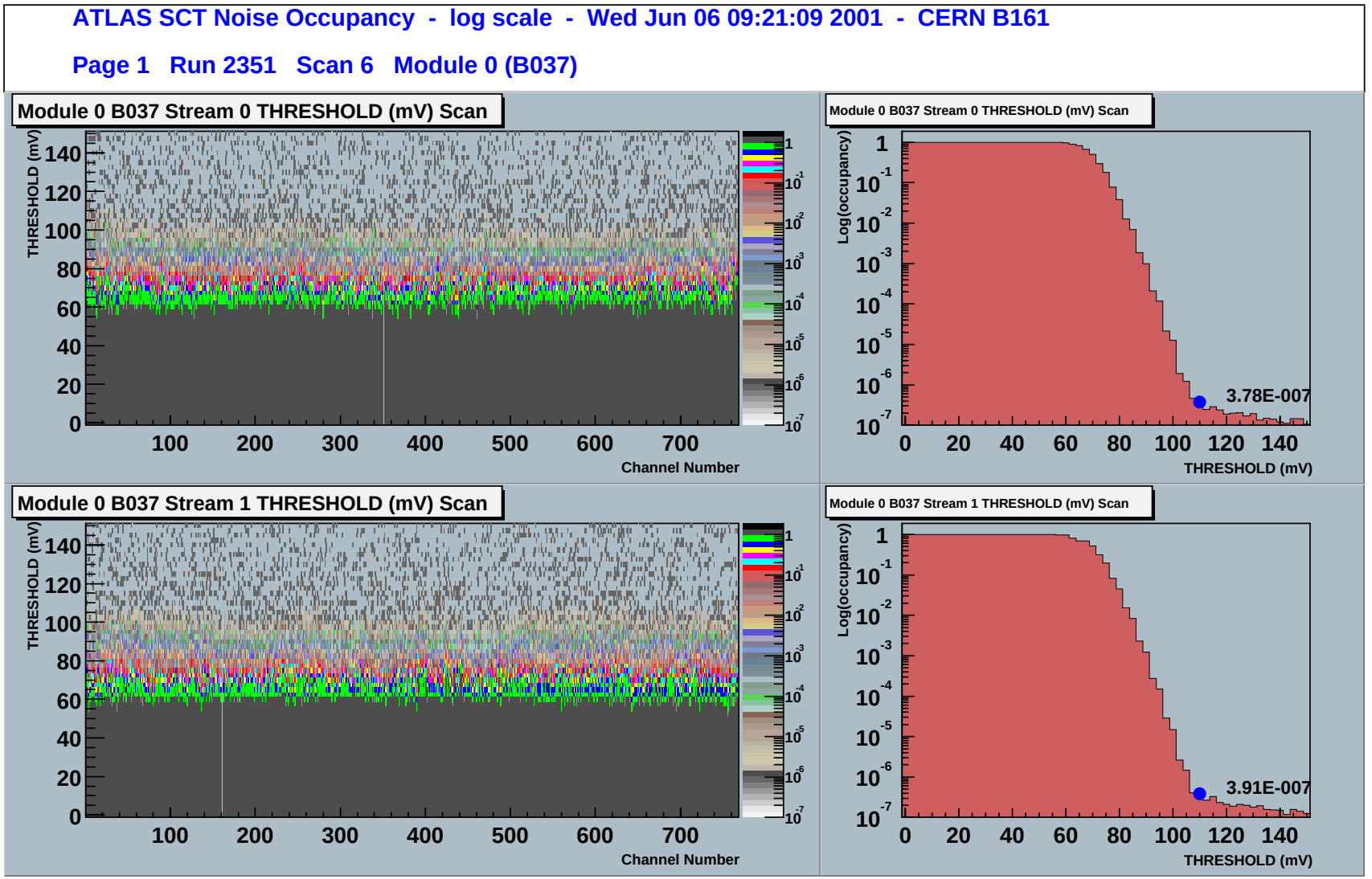

Figure 9: Measured noise occupancy versus threshold for each readout channel of module 20220170100037 after irradiation to $3x10^{14}$ pcm^{-2} (left-hand plots). The right-hand plots show the occupancy summed over all channels for each side of the module. The module is trimmed in range 2. (The indicated occupancy numbers are at an arbitrary threshold, and have no significance).

5 MODULE TEST-BEAM RESULTS

The modules as indicated in Table 1 have been tested in the H8 beam at CERN in August 2000 and in the KEK test beam in December 2000. The CERN test beam has the advantage of high momentum particles, a 1.56T magnetic field and the possibility of rotating the angle of the face of the silicon with respect to the incident tracks over the $\pm 20^{o}$ range relevant to barrel modules within ATLAS. However, only modules made with ABCD2T chips were available at the time of this test beam. The KEK test beam provides data from ABCD3T modules.

Both irradiated and non-irradiated modules have been measured in the beam tests. The modules are all kept cold, with the hybrids operating at about 0^{o}C. A beam telescope is used at both CERN and KEK to define the track positions at the module planes. SCT prototype power supplies are used, together with the MuSTARD readout system

Some principal results are briefly summarised in the following sections:

5.1 Charge Collection and Signal:Noise Ratio

The median charge of three modules, obtained from the 50% efficiency point in threshold scans, as a function of detector bias voltage from KEK data is shown in Figure 10.

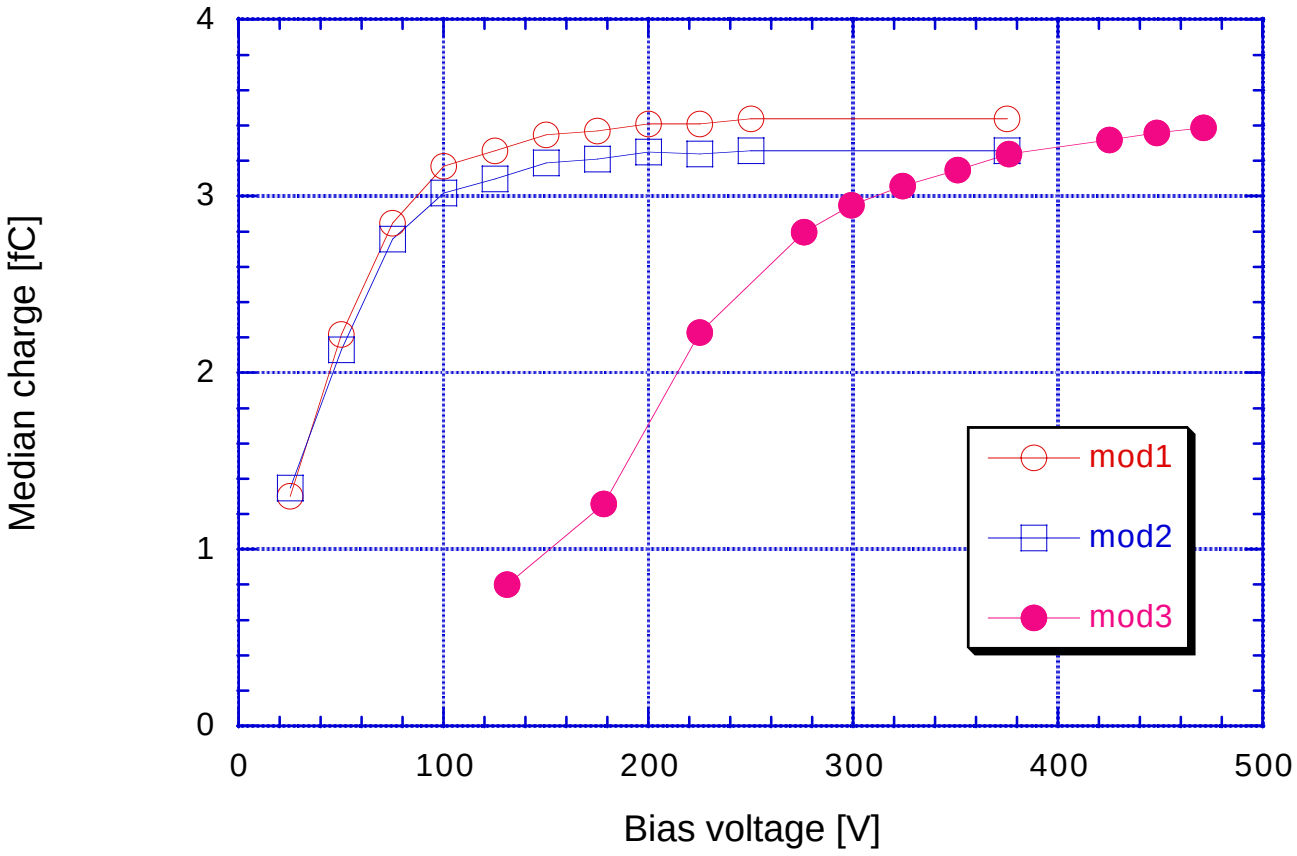

Figure 10: Median charge (fC) versus bias voltage for the ABCD3T modules 20220170100011, 22 and the irradiated module 20220170100003 (solid circles, mod3)).

The detectors of the two unirradiated modules have depletion voltages of ~80V, and are normally operated at ~150V bias. The irradiated module is operated at ~400V bias, at which point it is seen that the collected charge on a single strip is similar to that for unirradiated modules. This result has also been measured with our detectors readout by (unirradiated) analogue electronics in the laboratory during our detector QA procedures.

Uncertainties in the performance of the calibration circuitry can be eliminated by looking at the signal:noise values of these modules as measured in the KEK test beam. This is shown, again as a function of bias voltage, in Figure 11. The signal:noise values discussed in section 4 above are to be seen.

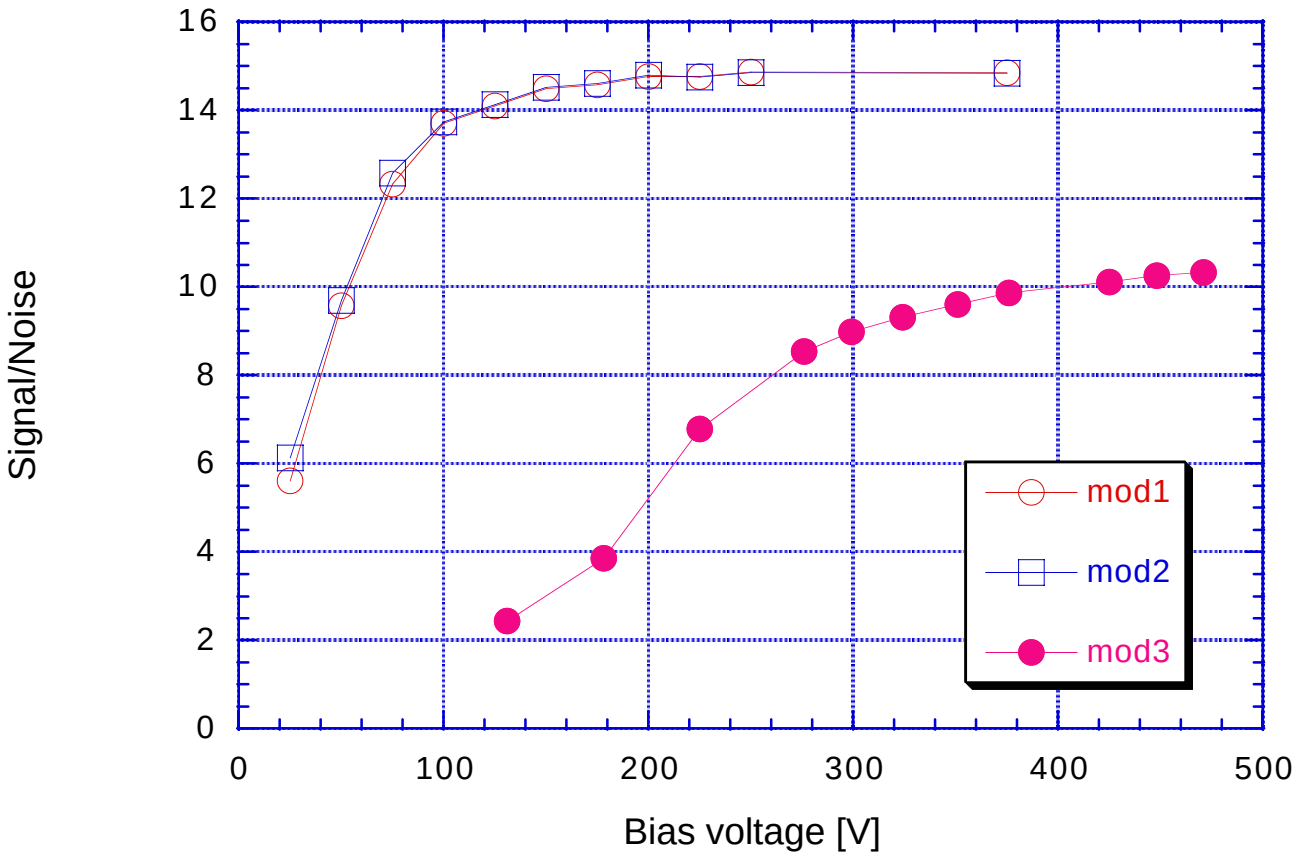

Figure 11: Signal:noise as a function of bias voltage for the same three modules as in Figure 9. Again, mod 3 is the irradiated module.

5.2 Efficiency at 1fC Threshold

The efficiency of the modules at the nominal operating threshold of the SCT is typically measured to be > 98% at the operational bias voltages over the full range of particle incident angles, with or without a magnetic field. This is illustrated by data from the CERN beam test. In Figure 12, the efficiency for an unirradiated module is shown as a function of angle, and in Figure 13 that of an irradiated module. (The maximum efficiency recorded is a function of tracking cuts, and plateau values in excess of 99% can be obtained).

These data give confidence that the modules will operate with high efficiency at 1fC threshold within the ATLAS environment.

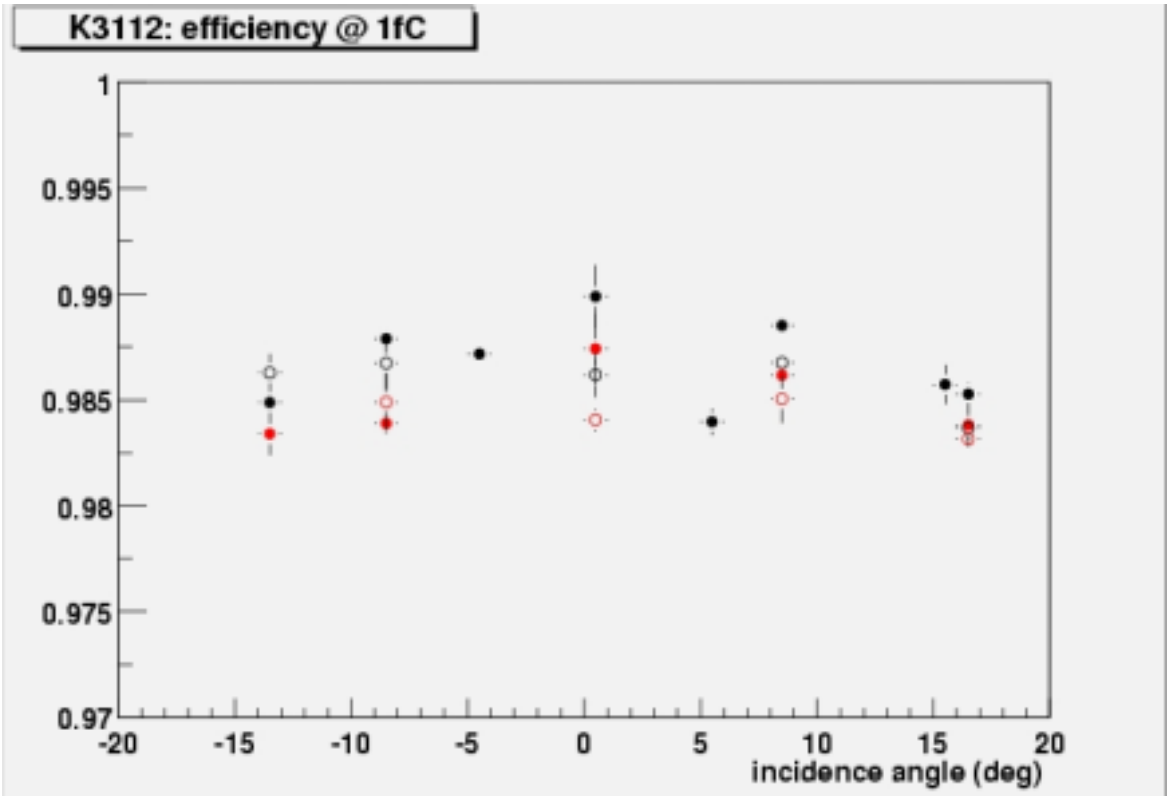

Figure 12: Measured efficiency of the unirradiated module K3112 at 1fC threshold as a function of the beam incident angle. The red symbols are with the magnetic field of 1.56T, the black with zero field. The open circles are with a bias voltage of 120V, the full circles with 200V bias.

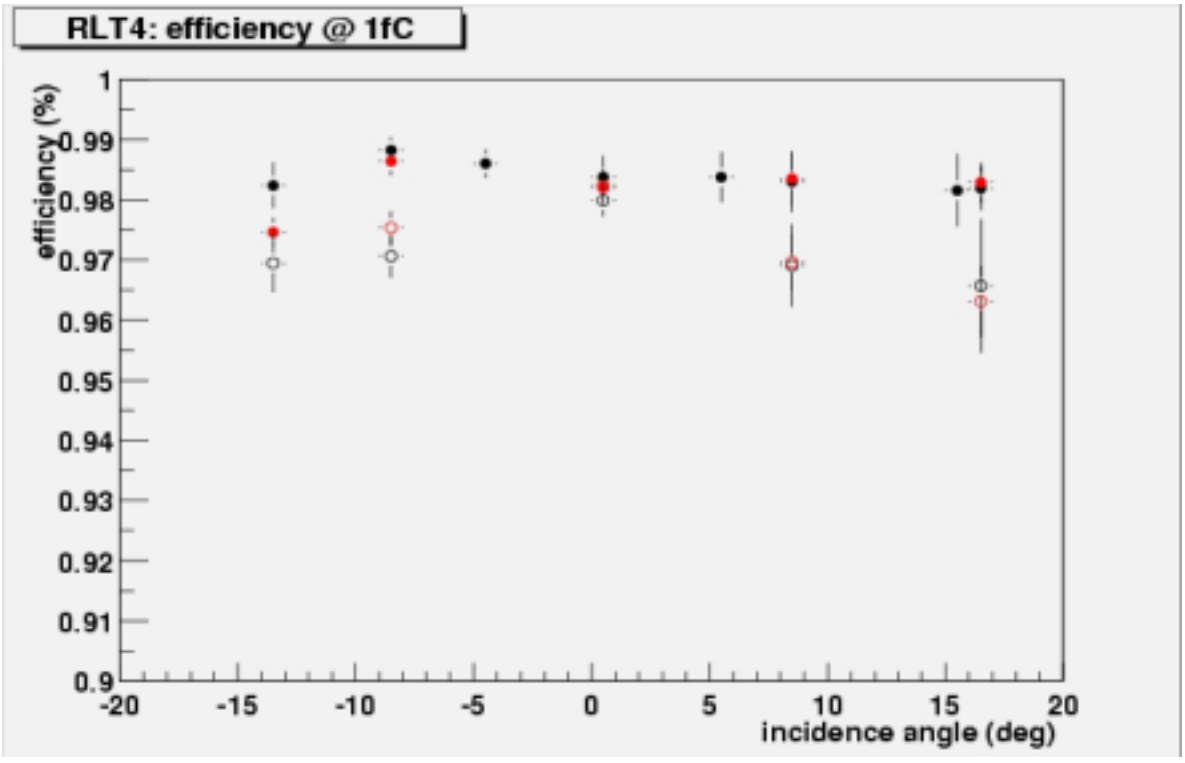

Figure 13: Measured efficiency of the fully irradiated module RLT4 at 1fC threshold as a function of the beam incident angle. The red symbols are with the magnetic filed of 1.56T, the black with zero field. The open circles are with a bias voltage of 300V, the full circles with 450V bias.

5.3 Resolution

The measured resolutions are consistent with the expectation of the 80μm binary strip pitch (ie 23μm). This is illustrated from the CERN beam test in Figure 14 for tracks at normal incidence, with the magnetic field on. The resolution for inclined tracks is slightly better because two strip clusters occur with greater frequency.

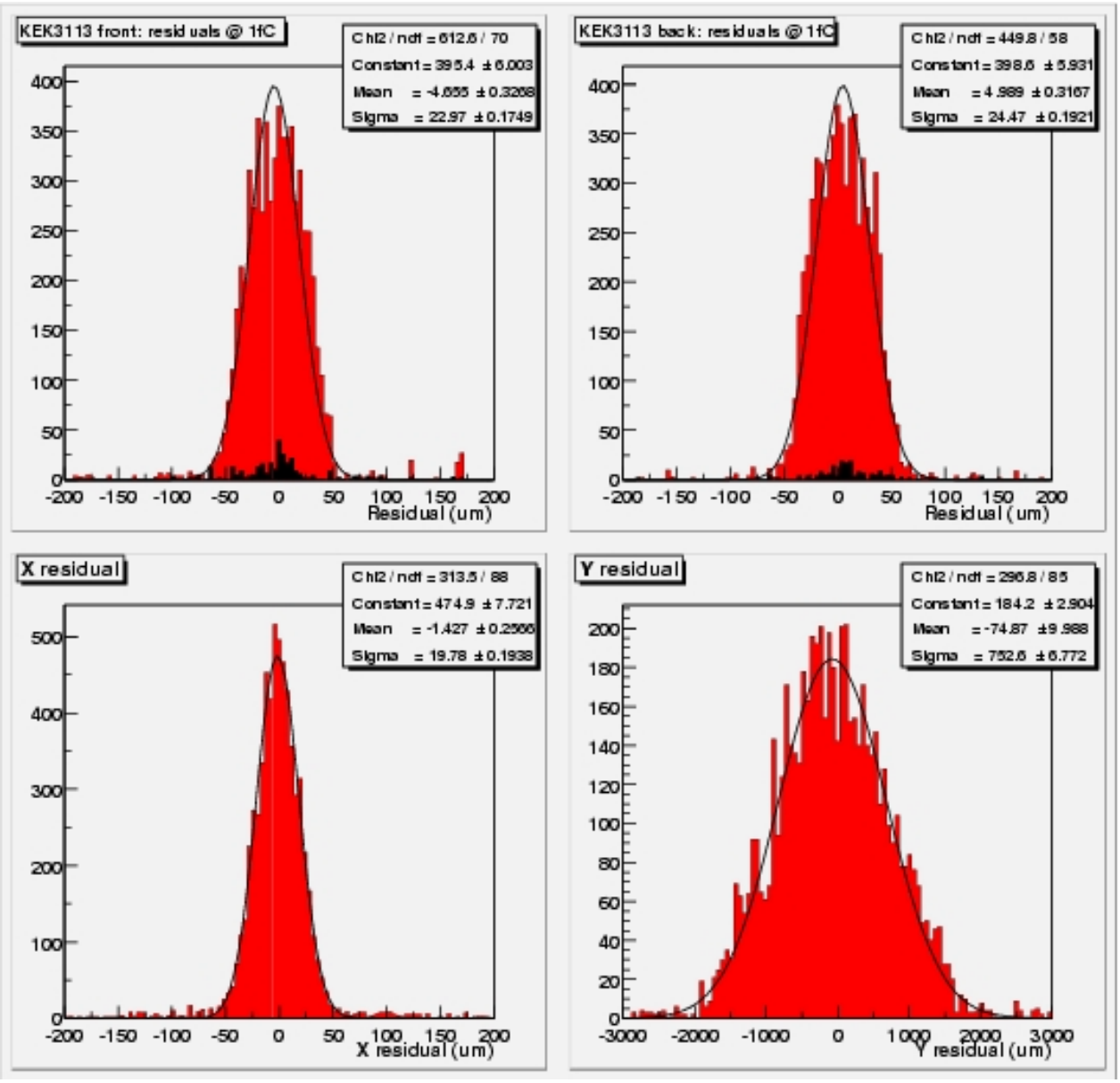

Figure 14: Reconstructed track residuals with the unirradiated module K3113. The top two plots show the u, v residuals of the two sides of the module (inclined at ±20mr), with the expected values of about 23 μm. The lower two plots show the reconstructed residuals in the x, y directions.

6 SYSTEM TEST AND FIRST RESULTS

6.1 General Description

The goal of the system test is to run as many modules as possible in a physical configuration which is as close as possible to the planned ATLAS SCT configuration, thereby testing the performance of the modules in such a system and comparing it to their stand-alone performance.

Modules are mounted on a sector of a Carbon-fibre-Corex-sandwich cylinder with dimensions very near to those of the innermost ATLAS SCT barrel. The sector can accommodate up to 48 modules, in four rows of 12.

Modules are powered and read out via prototype SCT barrel 'opto-harnesses', which transmit power to the modules, decode the optical clock and commands, transmit these signals electrically to the modules, and transform the data from the modules into optical signals for transfer to the readout electronics. Each opto-harness serves up to six modules, as in the final system.

The ASICs and opto-components are powered by the SCT prototype VME power supplies (SCTLVs); and the detectors are biased with the companion prototype high voltage units (SCTHVs).

The modules are read out using a CLOAC-SLOG-MuSTARD-OPTIF system, with the OPTIF[1] providing the electrical-optical interface. A further VME module is used to read module hybrid temperatures. The ROOT-based SCTDAQ software package is used, running on a Windows-NT PC which is connected to the VME crates via a National Instruments interface card.

Control and monitoring of all voltages and currents is currently carried out through the DAQ software, although a prototype DCS system is used to monitor environmental temperature and humidity.

All patch panels and power tapes used are true to the planned final ATLAS design, except for extra provisions on the patch panels to allow testing of various coupling schemes. The conventional cables used between PPB2 and the power supplies are 30 metres long The patch panel PP3 and the cables from PP3 to the power supplies, foreseen for the experiment, have not yet been simulated in the system test.

A schematic diagram of the system test can be seen in Figure 15 and photographs of the barrel sector can be seen in Figures 16 and 17.

6.2 Grounding and Shielding in the System Test

The system test bases its grounding and shielding scheme on the proposal outlined in *ATLAS SCT / Pixel Grounding and Shielding Note*[2]. The main elements as applied in the system test are described below, with any differences noted.

To control stray capacitance between the cooling pipe and the silicon detector backplane, shunt shields are placed between the modules and the cooling pipe. These shunt shields consist of copper on kapton; with the copper soldered to Analogue Ground on the 'dogleg' (the portion of the opto-harness to which the module is connected).

[1] http://s.home.cern.ch/s/sct/public/sctdaq/sctdaq.html

[2] http://scipp.ucsc.edu/groups/atlas/elect-doc/SCT_GND_SHIELD2.pdf

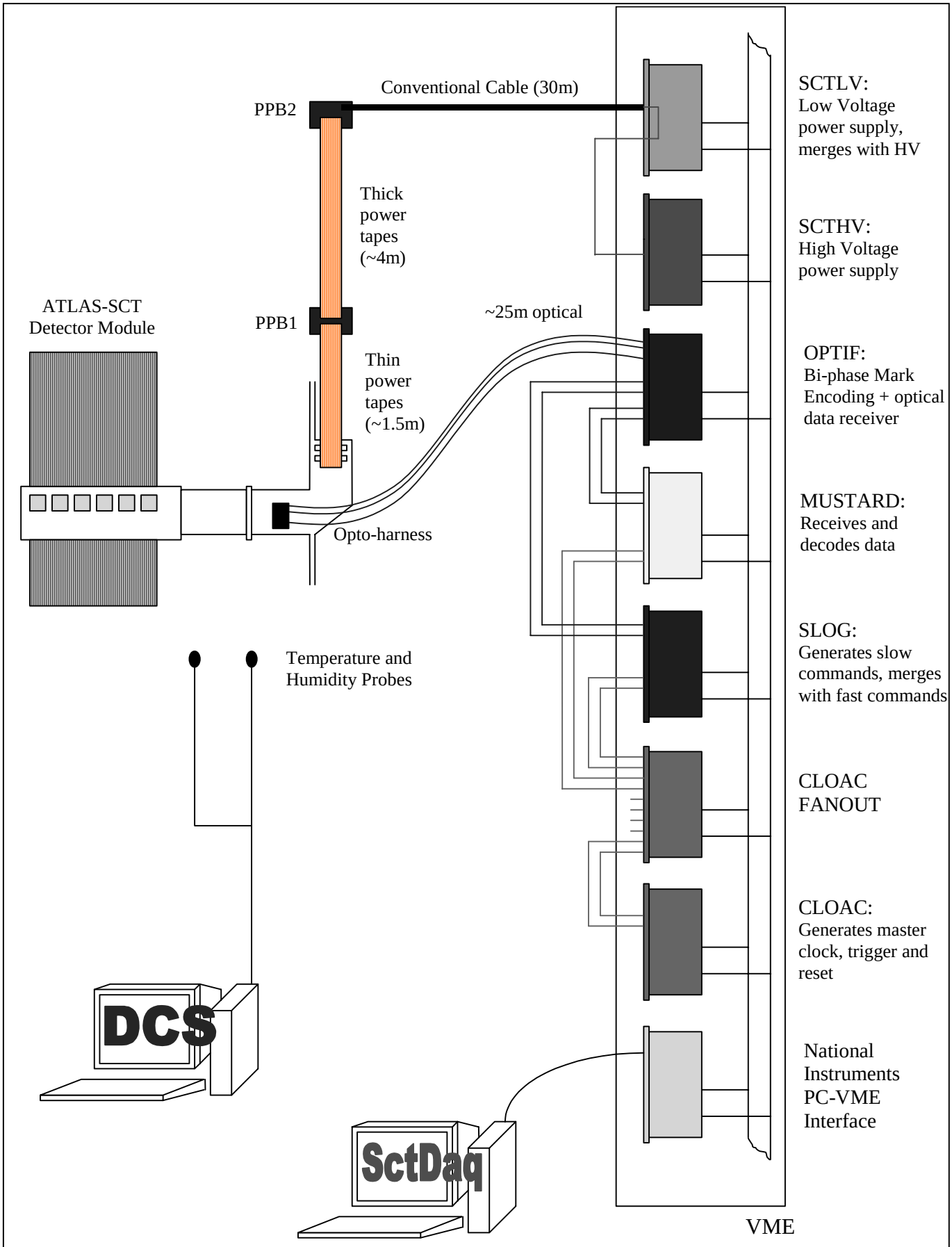

Figure 15: A schematic layout of the SCT barrel system test

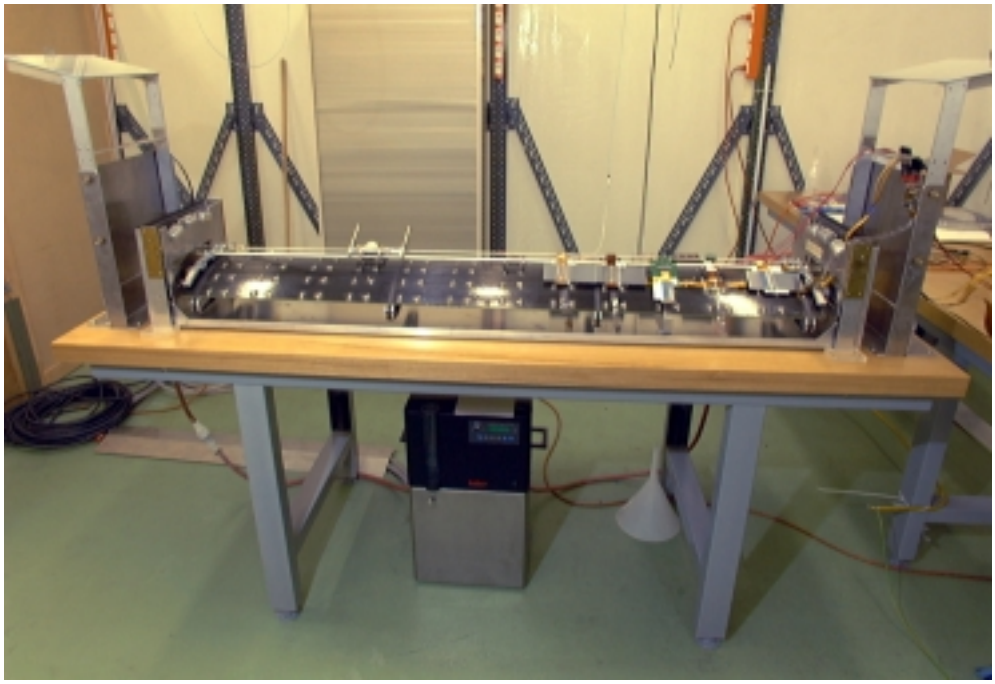

Figure 16: A photograph of the system test barrel carbon-fibre mounting structure

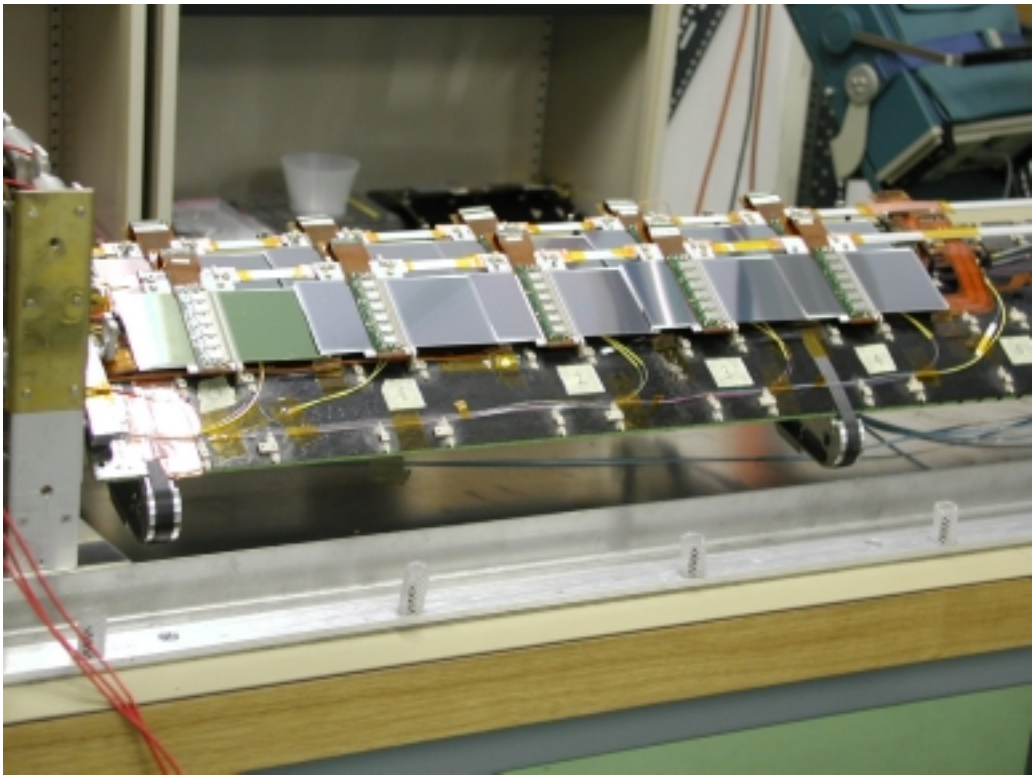

Figure 17: A photograph of barrel modules mounted on the carbon-fibre structure

The cooling pipes are connected together at both ends of the sector via an aluminium support bracket. This bracket is screwed onto the sector, providing electrical contact to the carbon fibre skin. Note that the cooling pipes are continuous, with no electrical break in the centre. The metalwork which supports the sector is also made of aluminium and is connected electrically to the sector by its contact with the carbon fibre skin. An aluminium cover (with square cross-section), used to provide a dry and light-tight atmosphere whilst running, is in electrical contact with the support structure. It should be noted that the cover is not electrically or geometrically similar to the planned ATLAS SCT thermal shield; a cover that will simulate the thermal shield is currently being produced.

Routing from the harness to PPB1, the six 'thin' power tapes from a harness are wrapped together with aluminium-on-kapton shielding which is DC-connected to the metalwork surrounding the sector. At PPB1, digital and analogue grounds are AC-connected (with 2.7 μF) to the cable shielding.

From PPB2 to PPB1, the system test is not very like the ATLAS SCT; there is no surrounding metal (e.g. heat spreader plates, cooling supply tubes) to connect to as is recommended in the note referenced above. For the 15-module tests reported below, all three set of six 'thick' power tapes running from PPB1 to PPB2 were wrapped with aluminium-foil shielding which was connected to grounds at PPB1 and PPB2 in the same way as described above for the thin tapes.

Common-mode chokes are used between PPB2 and the conventional cables. These chokes are intended for use at PPB3 but as stated above PPB3 is not (yet) represented in the system test.

The low- and high-voltage power supplies have floating grounds.

An alternative grounding and shielding scheme, which involves DC connections between all metal in the system and DC connection of the module grounds to the cooling pipe, is working well in the SCT-endcap system test but remains to be tested in the barrel system test.

6.3 First Results from the Barrel System Test

When a module arrives at the system test, it is accompanied by the results from a standard characterisation as performed at the module building cluster. The first step in integrating the module into the system test is to repeat this standard characterisation on the 'electrical test bench' in the system test lab, to verify that the module has not suffered in transit. The electrical test bench is considerably simpler than the full system test as it bypasses the optical communication, and uses only very short power and signal cables. Therefore a module may be expected to give its best performance when running stand alone 'on the bench'.

Once the module is verified to be in good working order, it is mounted on the system test sector (with all grounding and shielding connections made), and the standard characterisation sequence is repeated, powering only that one module. This performance is compared to that on the bench and any differences are noted and investigated if possible. When this comparison is complete, the module is considered ready to be included in multi-module tests.

There are currently 15 modules in the system test, as seen in Table 1. Thirteen of these are considered 'good' modules; the other two (20220170100004 and 9) are included on the sector to maximise the overlap of powered modules for these first results, until further modules are available.

A typical multi-module test which can be done is to measure the gain and noise with many modules running in parallel. This has been performed, using a three-point gain calculation, with the 15 modules on the sector. For this test there were three harnesses on the left-hand half of the

sector, mounted immediately adjacent to one another. From left to right on the front harness were modules 0035, 0036, 0022 and 0026, on the middle harness Scand1, K3112, K3104, 0011 and K3103; and on the back harness were 0029, 0018, 0019, 0008, 0009 and 0004. The measured noise values of all ASICs on the modules, with all 15 modules in operation at a hybrid temperature of about 27^0C, are shown in Figure 18. The noise values lie in the anticipated range.

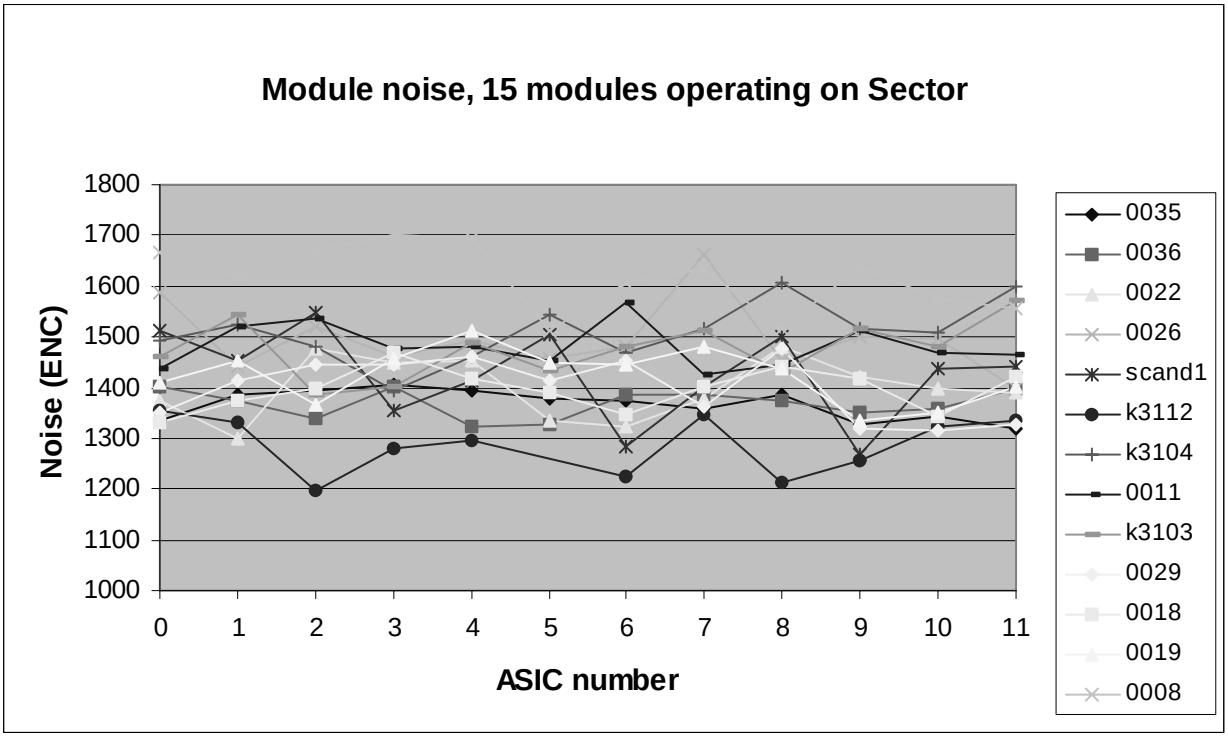

Figure 18: The measured module noise for each ASIC with 15 modules operating together on the barrel system test sector

The noise difference between this 15 module operation and that measured when a module is tested individually on the electrical test stand is shown in Figure 19 for each ASIC. The differences are seen to be below ~200 ENC in all cases.

Tests have begun on the longer-term stability of the 15 modules operating together on the sector. In Figure 20 the rms spread of the noise is shown, as derived from repeated 3-point gain scans over an 8 hour running period. Good stability is seen, with the maximum rms of only 15 ENC for any ASIC. In Figure 21, the average noise occupancy over the 8 hour period is shown, at a threshold of 1fC. All ASICs have a noise occupancy of less than $5x10^{-4}$, and those made with ABCD3T(-A) ASICs are below 10^{-4}.

Detailed studies continue, but these first results from the 15 module barrel system test are clearly encouraging.

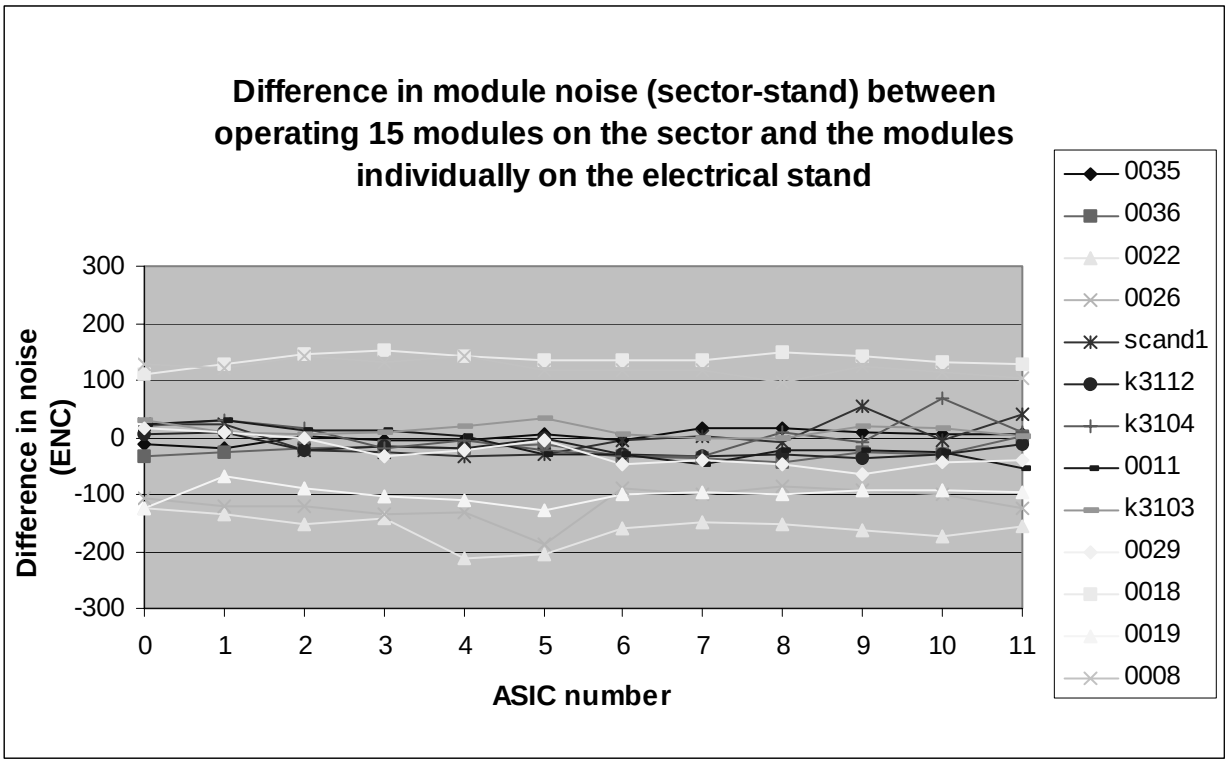

Figure 19: The change in the module noise between running with 15 modules on the sector and individual operation on the electrical test stand for each ASIC.

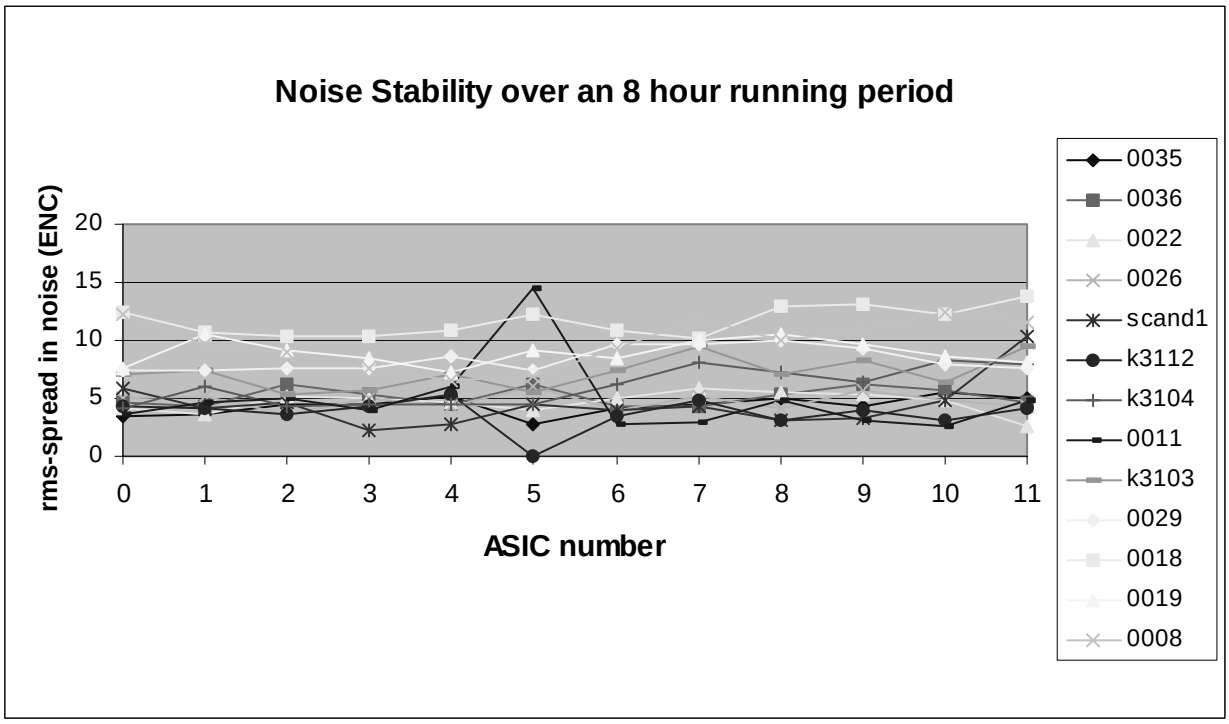

Figure 20: The rms spread of module noise for each ASIC derived from repeated measurements made over an 8 hour running period with 15 modules on the sector.

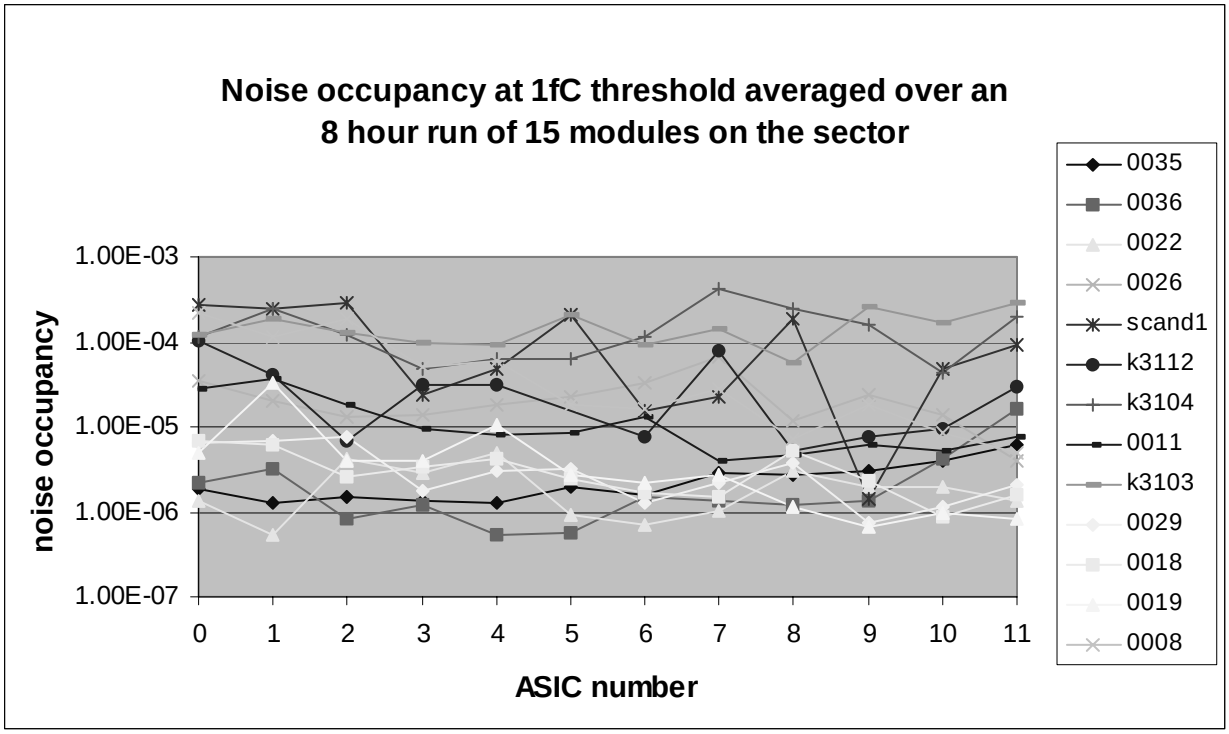

Figure 21: The average noise occupancy for each ASIC derived from repeated measurements made over an 8 hour running period with 15 modules on the sector.

7 SUMMARY

The SCT barrel modules satisfy the electrical performance goals of the ATLAS Inner Detector TDR, with the possible exception of a slightly higher final post-irradiation noise value. The modules operate in a stable fashion, with good efficiency and low noise occupancy at 1fC threshold. The first results from a collection of 15 modules running together in the SCT system test are encouraging.

The available data therefore indicate that the design of the barrel module, and all its components, adequately meet the electrical performance requirements of ATLAS.

APPENDIX 1 OUTLINE OF MODULE ELECTRICAL TESTS

An extensive suite of both hardware and software[1] has been developed to facilitate module testing. The readout system is based around the VME modules CLOAC, MuSTARD and SLOG. The prototype low voltage and high voltage modules, SCTLV and SCTHV, are also part of the system.

Two largely automated series of tests[2] have been devised to simplify the testing procedure, as outlined in Table 1. The *Characterisation Sequence* aims to perform the full characterisation of a hybrid or module whereas the shorter *Confirmation Sequence* provides a reduced set of information. The *Confirmation Sequence* ensures that the digital part of the ASICs is functioning, none of the critical wire-bonds have been damaged and that the basic analogue performance of a module has not deteriorated. It is anticipated that the *Confirmation Sequence* would be repeated at regular intervals during the long-term tests and each time that a hybrid or module is shipped between institutes.

	Characterisation	**Confirmation**
Power On Tests / Verification of Response to Hard Reset	√	
Clock and Command Reception Test	√	√
Bypass Functionality Test	√	√
Pipeline Efficiency Test	√	
Strobe Delay Scan	√	√
Three Point Estimation of Gain, Noise and Offset	√	√
TrimRange Scan	√	
Determination of the Response Curve	√	
Noise Occupancy Scan	√	
Timewalk Scan	√	

Table 1: The Characterisation and Confirmation Sequences

In general, the analogue performance of a module/hybrid is measured with respect to the internal calibration circuitry of the ABCD3T chip. Hence it is necessary to make a correction for the variation of the calibration capacitance between batches of ASIC wafers.

There follows a brief description of the individual tests to be performed as part of the electrical QA procedure. The description contains the method in general terms, the purpose of the tests and in quantitative terms the criteria for PASS/FAIL cuts. A summary of the results of each test will be recorded in the SCT database.

A module is classed as `good' if at least 99% of its readout strips will operate efficiently with low noise occupancy at 1fC threshold.

[1] http://sct.home.cern.ch/sct/sctdaq.html

[2] The tests are described fully in http://hepwww.rl.ac.uk/atlas-sct/documents/Electrical_Tests.htm

1. Power on Tests / Verification of Response to Hard Reset

The module/hybrid is clocked and the power is switched on. The operator must verify that each data-link responds with CLK/2 and that, after the chips have been configured, the clock feed-through signal stops. The analogue and digital currents are then recorded. Finally Hard Reset is issued to bring back the CLK/2 signal.

This test verifies that the Clock, Command and Hard Reset signals are received correctly, that the chips can be configured and that the current consumption is reasonable. The test will identify modules/hybrids with severe failures. Every module must pass this test without error.

This is the only test that would normally require operator intervention.

2. Clock and Command Reception / Addressing Error Test

The chips are configured to return the contents of the Mask Register and a burst of triggers is issued for each of the Primary and Redundant Clock and Command options. Prior to each event, a different bit pattern is loaded in the Mask Register such that consecutive events are not the same.

By comparing the received data with expectation it is verified that both the Primary and Redundant Clock and Command signals are received correctly and that the top address bit of each chip changes as the Clock/Command source is varied, as specified in the module design. This test will identify modules/hybrids with faulty command reception or addressing errors. Modules/hybrids with such defects would be considered to have failed pending further investigation and possible rework.

3. Bypass Functionality Test

A trigger burst is recorded with the module/hybrid programmed to each of a number of different configurations, sufficient to exercise all data/token passing links between the chips. In each case the chips are configured to return the contents of the Mask Register such that the expected data are accurately known. The test is repeated across a range of digital supply voltages.

This test determines the minimum value of the digital supply voltage needed for each of the data/token passing links to work. Any link that did not work at the designated supply voltage, and which could not be identified as being due to a missing wirebond and subsequently repaired, would cause a module/hybrid to be rejected.

4. Pipeline Efficiency Test

For this test, a Soft Reset command is sent to reset the pipeline followed a certain number of clock periods later by a Pulse Input Register command and L1A trigger. In this way, a known pattern is injected into a given location in the pipeline. By varying the distance

between the Soft Reset and Pulse Input Register commands it can be verified that each of the eleven blocks within the pipeline is free of defects.

Zero occupancy for a particular number of clock periods between the Soft Reset and Pulse Input Register commands would indicate a dead cell in the corresponding block of the pipeline. Zero occupancy for all values would indicate a dead channel. Modules/hybrids with a large number of dead Pipeline cells or dead channels will be rejected.

5. Strobe Delay Scan

This scan is performed to determine the correct Strobe Delay setting, corresponding to the timing of the charge injection pulse, to be used during the Analogue Tests.

6. Three Point Estimation of Gain, Noise and Offset

Threshold scans are taken for three injected charges to facilitate a quick measurement of gain, noise and the discriminator offset. Pathological channels are categorised as FAULTY if the defect would result in the channel having a reduced but non-zero detection efficiency in ATLAS, or as LOST if the defect would result in the channel having zero efficiency:

- Lost: Dead, Stuck, Unbonded or Noisy channels
- Faulty: Inefficient, Low Gain or Partially Bonded channels

Modules/hybrids having any chips with abnormal gain or high noise will be rejected, for potential re-work, as will those with large numbers of pathological channels.

7. Trim Range Scan

For each of the four possible TrimRange settings, a series of Threshold scans are performed for a subset of the sixteen possible TrimDAC settings, all with 1fC injected charge. For each TrimRange setting a straight line is fitted to the data for each channel to characterise the TrimDAC response and to determine the TrimDAC slope. The number of trimmable channels and the spread of the resultant trimmed thresholds are also recorded. The optimised TrimDAC settings and a list of channels to be masked are produced for use in the subsequent analogue tests.

The chips used to build modules will have been selected such that all channels may be trimmed using the smallest TrimRange. Modules which do not meet this specification on at least 99% of channels will be rejected, for potential rework, as will those where a particular TrimRange has a slope other than that expected.

8. Response Curve

Threshold scans are performed for a series of input charges and, for each channel, an appropriate function is fitted to the resulting response curve. From this the Gain, Noise and discriminator Offset are extracted.

The parameters from the fit are stored since they describe the correspondence between the Threshold, in mV, and input charge, in fC. The categorisation of pathological channels is repeated as described for the Three Point Gain. Modules/hybrids with a large number of pathological channels will be rejected.

9. Noise Occupancy Scan

A high statistics Threshold scan is performed at the nominal ATLAS trigger rate of 100kHz, without any injected charge, to determine the Noise Occupancy of each channel as a function of Threshold. The analogue and digital current consumption as a function of Threshold is recorded.

Channels with high Noise Occupancy will be added to the list of masked channels.

10. Timewalk Scan

This test performs a series of Strobe Delay scans with the Threshold set to 1 fC, varying the input charge from 1.25 to 10 fC. In each case a fit is made to the rising edge of the pulse to determine the Strobe Delay value needed to obtain 50% occupancy.

The Timewalk is defined as the time variation in the crossing of a threshold of 1fC over a signal range of 1.25 to 10.0fC. This parameter is calculated and recorded.